

1200V RC-IGBT based on CSTBTTM with Suppressed Dynamic C_{res} and Partial Lifetime Control

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Abstract— In this paper, a newly developed low loss RC-IGBT is presented. In order to reduce the power loss of RC-IGBTs, we introduced two approaches. One is an optimization of dynamic feedback capacitance that induces a voltage tail and an increase of power losses. Another approach is a lifetime control technique for the RC-IGBT without adverse effect on the characteristics of the IGBT. The proposed 1200V RC-IGBT based on CSTBTTM realizes a 29% reduction in DC loss and a 4% reduction in AC loss by using suppressed dynamic C_{res} , a Partial lifetime control, in addition to our thin wafer technique.

Keywords—RC-IGBT; Voltage tail; Miller Capacitance (C_{res}); Lifetime Control

I. INTRODUCTION

There are strong demands for the miniaturization and high power density of power modules. A Reverse Conducting – Insulated Gate Bipolar Transistor (RC-IGBT) has attracted great attention as a device to contribute to these demands. The RC-IGBT brings the benefits of reducing the number of components, downsizing, and heightening the power density by comprising the IGBT and diode into a single chip. The total power loss of the RC-IGBT has been improved by the progress of thin wafer technique and optimizations of the layout and structure [1-3]. The RC-IGBT has been utilized in home appliances, industrial motor drives and electric vehicles. Accordingly, it is important to optimize the performance of the RC-IGBT for each usage condition. We have been developing technologies for the RC-IGBT to adapt to the various usage conditions.

The RC-IGBT can reduce thermal resistance and temperature ripple because of the chip layout which has the IGBT and diode elements adjacent to each other as shown in figure 1. Therefore, a higher current density can be applied to the RC-IGBT than when the IGBT and diode are separate. However, there is the problem that the high current density causes a “Voltage tail” during switching operation as shown in figure 2. In particular, under the usage condition with a high gate resistance (R_G) to satisfy the strict upper limit of di/dt or dv/dt , the voltage tail increases power consumption drastically. Though there is a way to suppress it by using an extra circuit [4], it is preferable that the voltage tail is suppressed by the optimization of the device structure.

Another problem is the way to control the Reverse Recovery Current (I_{rr}) in the RC-IGBT. We fabricated the anode of the diode by a common process with the IGBT to reduce the increasing wafer process. Therefore, the diode element has a high doped Anode diffusion layer which causes a large I_{rr} . For the conventional RC-IGBT, Entire Life time Control (ELC) with an irradiation of an Electron Beam (EB) or light ion is used to control the I_{rr} . However, the controlled lifetime layer in the IGBT element causes the degradation of the IGBT characteristics [3]. In this work, we analyze the mechanism of the voltage tail, and propose the structure to suppress it as a first approach. The second approach is a Partial Lifetime Control (PLC) [5] as a method to control the I_{rr} without the degradation of IGBT characteristics. In addition to these approaches, the high avalanche capability structure reported in ISPSD2018 [1] and the thin wafer technique are combined. As a result, the proposed 1200V RC-IGBT realizes a drastic reduction of total power loss.

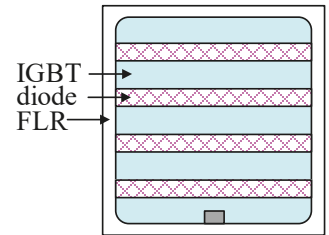


Fig. 1. RC-IGBT chip layout example

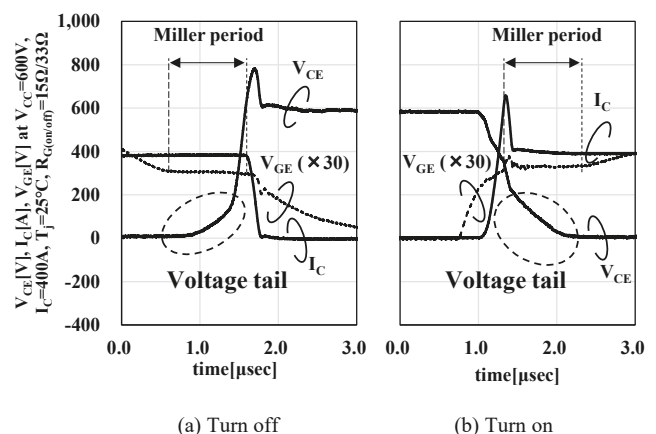


Fig. 2. Conventional switching waveforms containing voltage tail

II. DEVICE STRUCTURE

Figure 3 shows the conventional and proposed structures. In the conventional structure, the IGBT element has a CSTBTTM structure with a n-carrier stored layer (CS-layer) underneath the

	Conventional structure	Proposed structure
Cross-sectional view		
Features	<ul style="list-style-type: none"> •Narrow Trench pitch •Active trench ratio 1/4 (1 Active + 3 Dummy) •Entire Lifetime Control (ELC) 	<ul style="list-style-type: none"> •Wide Trench pitch •Active trench ratio 3/6 (3 Active + 3 Dummy) •Partial Lifetime Control (PLC) •Thin wafer thickness

Fig. 3. Cross-sectional views and features of conventional and proposed structure.

p-base and narrow pitch trench gates. Active trenches and dummy trenches are arranged, where the dummy trenches are connected to the emitter. The ratio of the active trench to dummy trench is 1/4 (1Active+3Dummy). The diode element of the conventional structure has the common p-base, p⁺-contact, CS-layer and dummy trenches, the same as the IGBT element in order to avoid the additional processes. In addition, the Lifetime Control layer is formed through the entire IGBT and diode elements by using ELC.

On the other hand, the proposed IGBT element has a wider trench pitch than the conventional type. The ratio of active trench to dummy trench is 3/6 (3Active+3Dummy). The channel densities of the conventional and proposed structures are adjusted to approximately the same by arranging the n⁺-emitter pattern. Lifetime control is performed only in the diode element, which we call PLC. The PLC is done by light ion irradiation through a patterned metal mask. The metal mask interrupts irradiated ions at the IGBT region, and creates a short lifetime control layer of silicon bulk, only in the diode. The wafer thickness of the proposed structure is thinner than the conventional structure.

III. SIMULATION ANALYSIS OF VOLTAGE TAIL

Generally, the dv/dt of the switching operation has an inverse relationship with R_G and feedback capacitance (C_{res}) as expressed in the equation below.

$$dv/dt \propto 1 / (C_{res} \times R_G) \quad (1)$$

During the voltage tail, the dv/dt becomes small even though the R_G is constant. Accordingly, we consider that the voltage tail is caused by an increase of C_{res}. Moreover, the behavior of dynamic C_{res} under the Miller period is important because the period of the voltage tail occurs during the Miller period (Fig. 2.). To analyze the increase of the C_{res}, we simulated the C_{res} at (1) V_{GE} = 0V as the normal C_{res} condition, and (2) V_{GE} = 10V as simulating the Miller period condition, with conventional and

proposed trench arrangements. The simulation models had the same conditions of lifetime and drift thickness. Figure 4 shows the simulation results. In the case of (1) V_{GE} = 0V, There is no special behavior in either structures. However, in the case of (2) V_{GE} = 10V, an increase of C_{res} is observed in the conventional trench arrangement while the V_{CE} is less than 400V. We can conclude that the voltage tail is induced by this behavior of C_{res} and named it as Dynamic C_{res} (D-C_{res}).

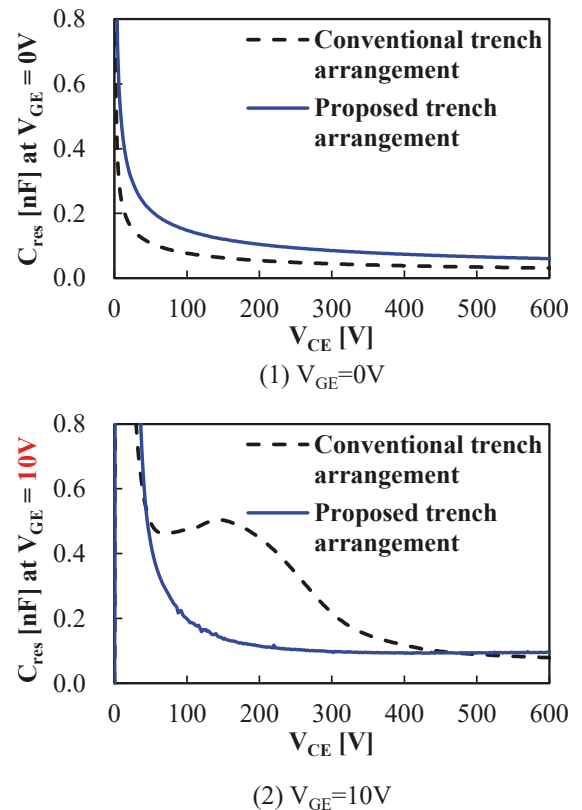


Fig. 4. Simulation results of C_{res}.

Figure 5 shows the relationship between the simulated electric potential under the active trench (V_{tr}) and V_{CE} . Figure 6 shows the simulated electric potential distributions at $V_{GE}=10V$, $V_{CE}=200V$ condition. C_{res} becomes smaller by the depletion layer generated under the active trench when the electric potential of V_{tr} becomes higher than V_{GE} . In the conventional trench arrangement, V_{tr} rises gradually because of the close dummy trench connected to the emitter. As a result, the $D-C_{res}$ becomes large up to $V_{CE}=400V$ and the voltage tail is induced by the large C_{res} .

In contrast, the proposed trench arrangement has the wide trench pitch which reduces the influence of the dummy trench. In addition, the consecutive active trench arrangement reduces the active trench's area facing the dummy trench. As a result, C_{res} becomes small due to the rapid rise of V_{tr} .

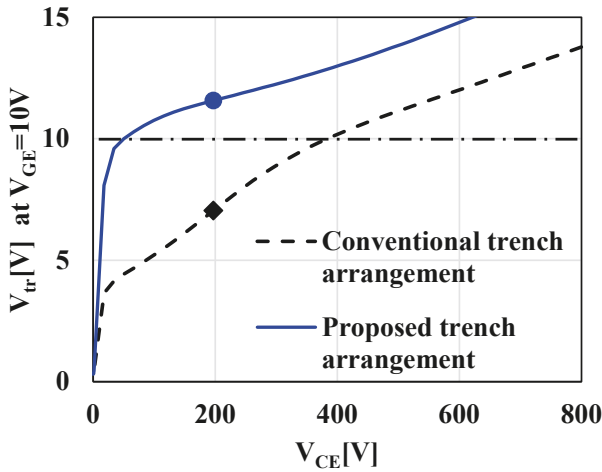


Fig. 5. Simulation results of relationship between V_{tr} and V_{CE}

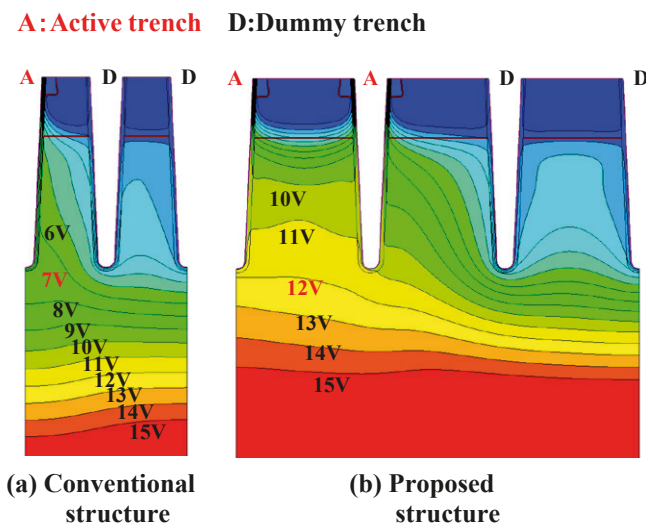


Fig. 6. Simulated electrical potential distributions around trenches of IGBT at conventional and proposed structure ($V_{GE}=10V$, $V_{CE}=200V$).

IV. EXPERIMENTAL RESULTS

We fabricated several RC-IGBTs with suppressed $D-C_{res}$ and PLC to demonstrate the effects of these techniques. At first, Figure 7 shows the experimental $V_{CEsat}-E_{off}$ trade-off relationship of the RC-IGBT with ELC or PLC. The samples had the conventional trench arrangement and drift thickness. In addition, the sample of PLC had a changed p-collector concentration. By forgoing the lifetime control layer only in the IGBT element, V_{CEsat} and E_{off} were reduced by 27% and 6%, respectively.

Secondly, we demonstrated the effect of the proposed trench arrangement on suppressing the $D-C_{res}$ and voltage tail. Figure 8, 9 and 10 show the experimental turn-off, turn-on and reverse recovery waveforms of the samples with conventional and proposed trench arrangements, respectively. The samples applied PLC and thin wafer thickness. The voltage tail becomes smaller with the proposed trench arrangement suppressing $D-C_{res}$, therefore it is able to reduce the E_{off} by 6% as shown in table 1. The suppressed $D-C_{res}$ and voltage tail produces a steep increase of voltage under the reverse recovery behavior. Therefore, the reverse recovery loss (E_{rec}) increases due to the suppressed $D-C_{res}$. However, the proposed structure is able to reduce $E_{on}+E_{rec}$ by 16% because the reduction of E_{on} is larger than the increase of E_{rec} .

Finally, figure 11 shows the trade-off between the DC loss ($V_{CEsat}+V_F$) and the AC loss ($E_{off}+E_{on}+E_{rec}$) of four kinds of RC-IGBT with (a) conventional structure, (b) applied PLC, (c) applied PLC & thin wafer, (d) applied PLC & thin wafer & suppressed $D-C_{res}$ (proposal). The proposed structure achieves a 29% reduction in DC loss and a 4% reduction in AC loss compared with the conventional structure.

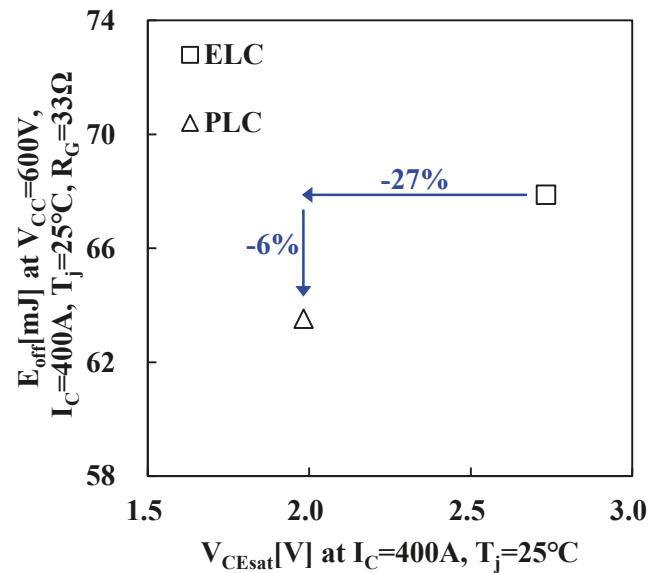


Fig. 7. Experimental results of $V_{CEsat}-E_{off}$ trade-off with ELC or PLC

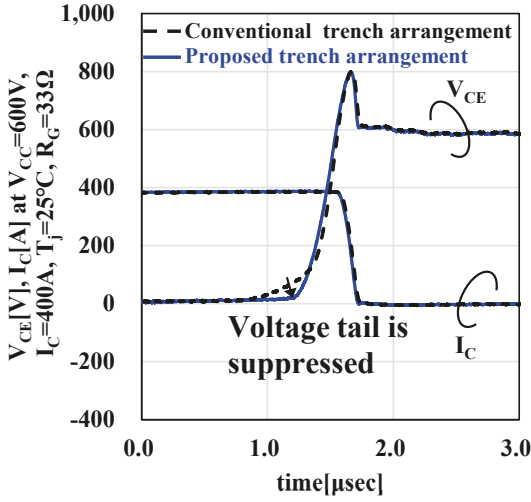


Fig. 8. Experimental switching waveform (Turn-off) with conventional and proposed trench arrangement

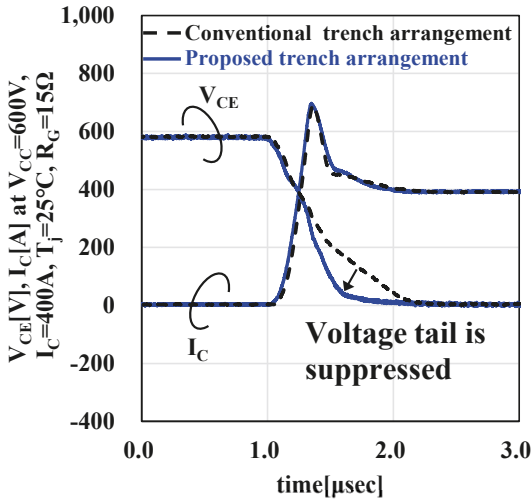


Fig. 9. Experimental switching waveform (Turn-on) with conventional and proposed trench arrangement

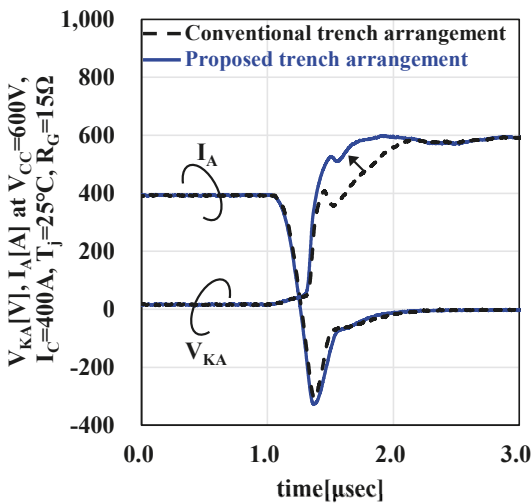


Fig. 10. Experimental Reverse Recovery waveform with conventional and proposed trench arrangement

TABLE 1. Experimental results of power losses with conventional and proposed structure

	E_{off}	E_{on}	E_{rec}
Conventional trench arrangement	64mJ	78mJ	23mJ
Proposed trench arrangement	60mJ	53mJ	32mJ
Reduction	6%	16%	

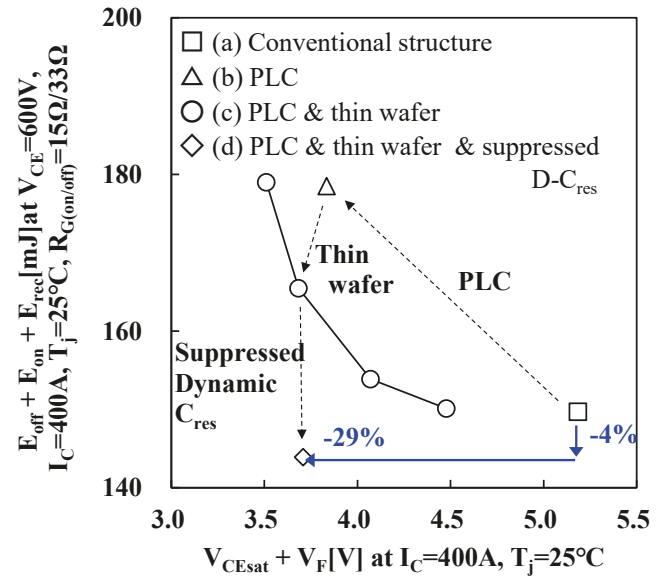


Fig. 11. Experimental results of trade-off between $V_{CEsat}+V_F$ and $E_{off}+E_{on}+E_{rec}$

V. CONCLUSION

We found that the voltage tail during the IGBT switching operation is induced by Dynamic C_{res} and succeeded to reduce it with a new trench arrangement. Moreover, we showed that Partial lifetime control is a suitable technique for the RC-IGBT to improve IGBT characteristics. Therefore, we have demonstrated the improvement of total power losses of the 1200V RC-IGBT based on CSTBTTM, drastically by these techniques.

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